REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

This Amendment is in response to the Office Action dated October 25, 2005. By the present amendment, the previously pending claims 1-4 have been canceled without prejudice to the applicants right to proceed with the subject matter of these claims in a continuation application. In their place, new claims 5-16 have been added to clarify the invention, as will be discussed below.

Briefly, the present invention is directed to an improved semiconductor integrated circuit device which can be used, for example, to provide an improved system arrangement utilizing a peripheral LSI to transfer data between a CPU and peripheral devices. As discussed in the background of the invention on pages 1 and 2, peripheral LSIs (hereinafter PLSI) have been used in recent years with CPUs in systems such as cell phones, digital still cameras etc. However, as discussed on page 2, line 10 et seq., in the past, the whole semiconductor device including the PLSI makes up one CPU core memory space. Therefore, as discussed on page 2, line 20 et seq., this requires combining the CPU memory space and the PLSI memory space.

The present invention is directed to providing separate independent memory space for the CPU core and the PLSI, as discussed on page 2, line 23 et seq. In other words, two separate memory spaces are provided that are transparent to one another (page 3, line 5 et seq.).

Referring to Fig. 2, an overall arrangement with, for example, a cell phone is shown with a CPU 27 coupled to a PLSI 33. Details of the PLSI 33 are shown, for

example, in Fig. 1. As can be seen, the PLSI includes a flexible bus controller FBSC 22.

Fig. 3 shows a more detailed version of the FBSC 22. As can be seen, this FBSC includes an address translation circuit ACON and a first protocol decode and generation circuit CPAG and a second protocol decode and generation circuit PPAG. Fig. 4 shows an address translation for mapping between the PLSI 33 memory space MAB and the CPU 27 memory (MAC). Fig. 5 shows a more detailed construction of the address translation circuit ACON itself. With regard to this, it is important to note that, in accordance with the present invention, the address translation circuit ACON is formed separate from the CPU 27, for example, in this embodiment by being formed as part of the flexible bus controller FBSC 22,

As discussed on page 9, line 1 et seq., the flexible bus controller FBSC 22 uses the address translation information from the address translator ACON to map the memory space of the CPU 27 and the PLSI 33. As noted above, Fig. 4, which is discussed beginning on page 16, provides an illustration of an address translation between the PLSI 33 memory space MAP and the CPU 27 memory space MAC. For example, in an address translation operation between MAB and MAC, a start address CA1 in the CPU memory space MAC corresponds to a start address PA1 in the PLSI memory space. An address width RG1 is specified for the address within the CPU 27 memory space MAC. With regard to this, it is noted that a nonvolatile memory IFLS shown in Fig. 3 is provided to store the address information regarding a relationship between the CPU memory space and the PLSI memory space.

The advantage of the above discussed structure, with the address translation circuits ACON being provided independent of the CPU 27 (contrary to the Prior Art in

which the address translation arrangements are provided within the CPU itself), is that the address transformation is performed with specific hardware, rather than within the CPU itself. This is more advantageous in terms of meeting the need for high speed data processing because the data transfer can take place without intermediation (e.g., see page 11, lines 9-16.). As noted there:

> "The bus master here is a functional module like the CODEC circuits GRP which perform data processing. This is because data transfer without intermediation of the on-chip CPU 6 is more advantageous in order to meet the need for high speed data processing."

In addition, the arrangement of the invention enables access to another memory space without a complicated process such as program modification, thereby reducing the system development costs. This is discussed, for example, on page 12, line 20 et seq.

Reconsideration and allowance of the newly added claims 5-16 over the prior art and double patenting rejections based on the cited Prior Art to Takeda (USP 6,292,851), the Uffenbeck text, Cupps (U.S.2003/0226044), and Honmura (USP 6,845,496) is respectfully requested, whether considered alone or in combination with each another or cited Prior Art in this case. In each case, the independent claims 5, 7, and 15 define an arrangement having a first CPU which accesses a first memory space with address translations and a second memory space without address translations, an address translation circuit, a nonvolatile memory to store address information indicating a relationship between an address of the first memory space and an address of the second memory space, a first protocol decode and generation circuit connecting to a first bus connected to the first memory space and a second protocol decode and generation circuit connected to a second bus connected to a second bus connected to the second memory space, wherein the

address translation circuit is connected to the first and second protocol decode and generation circuits and comprises a register and an address calculation circuit. As such, it is clear from each of these independent claims 5, 7 and 15 that the address translation circuit represents a separate circuit element from the first CPU. In addition, each of the independent claims 5, 7 and 15 clearly defines the relationship between the first CPU, the address translation circuit, the nonvolatile memory and the first and second protocol decode and generation circuits for implementing the transfer of data with a translation from the address translation circuit between the first and second memory spaces. With regard to this, independent claims 5 and 7 contain significant further limitations regarding the operation of the recited circuit elements for implementing the translations between the first and second memory spaces. Claim 15 specifically defines a peripheral LSI separate from the first CPU to transfer the data between the first CPU and a peripheral device, where the peripheral LSI includes the address translation circuit, the nonvolatile memory and the first and second protocol decode and generation .

It is respectfully submitted that none of the cited references teach, suggest or claim this overall combination of features defined in the independent claims 5, 7 and 15, or their respective dependent claims. In the primary reference to Takeda, for example, from column 5, lines 42 to 44, column 6, line 1-4 and column 6, lines 62-65 it is indicated that the address translation in Takeda is actually performed in the CPU, not by separate circuit elements. For example, in column 6, lines 66 et seq.., it is stated:

> "The CPU 22, however, converts the changeable physical addresses to predetermined memory addresses, so that the alarm information is stored at fixed consecutive addresses in A-B-C order in the SDRAM 32."

As such, clearly Takeda fails to teach or suggest the claim structure of an address translation circuit, separate from the first CPU, defined in each of the independent claims 5, 7 and 15. With regard to this, none of the cited secondary references provide any teaching whatsoever which would suggest the complete modification of Takeda which would be necessary to provide an address translation circuit as defined by the present claims, rather than performing the address translation within the CPU itself. Therefore, reconsideration and allowance of the independent claims 5, 7 and 15 is respectfully requested.

Reconsideration and allowance of the dependent claims 6, 8-14 and 16 is also respectfully requested. In each case, these dependent claims define further specific features of the claim structure and/or operation which clearly are neither taught nor suggested by Takeda nor any of the other cited Prior Art references in this application ,whether considered alone or in combination with one another. Therefore, particular consideration and allowance of these dependent claims is also respectfully requested.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37

CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus, LLP Deposit Account No. 01-2135 (Docket No. 501.42810X00), and please credit any excess fees to such deposit account.

Respectfully submitted,
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